Claims

[c1] 1.A CMOS image sensor device comprising:

a substrate having an isolation structure that defines an active region;

a photodiode sensing region located in the substrate;

a reset transistor located on the active region of the substrate, wherein the reset transistor has a source region connected to a part of the photodiode sensing region; and

a buried contact, wherein a first end of the buried contact is located on the substrate between the photodiode sensing region and the reset transistor and extended over the isolation structure to cover the periphery of the isolation structure and electrically connect the source region of the reset transistor, and wherein a second end of the buried contact is located on the active region of the substrate to be used as a gate of a source follower transistor.

[c2] 2.The CMOS image sensor device of claim 1, wherein the photodiode sensing region is located under the isolation structure.

[c3] 3.The CMOS image sensor device of claim 1, wherein a spacer is formed on a sidewall of the buried contact.

[c4] 4. The CMOS image sensor device of claim 1, wherein the photodiode sensing region further comprises a doped region with the same conductivity as the source region of the reset transistor.

[c5] 6.The CMOS image sensor device of claim 1, wherein a P type well is further formed under the reset transistor.

[c6] 7.The CMOS image sensor device of claim 1, wherein the substrate is a first type conductivity substrate and the photodiode sensing region comprises a second conductivity doped region.

[c7] 8.The CMOS image sensor device of claim 1, wherein the substrate is a P type substrate, and the photodiode sensing region comprises a deep N type well.

[c8] 9.A process for producing a CMOS image sensor device, comprising:

providing a substrate;

forming an isolation structure in the substrate to define an active region;
forming a first well with first conductivity in the active region of the substrate;
forming a second well with second conductivity under the isolation structure in the substrate;
forming a gate dielectric layer over the substrate;
forming a first conductive layer over the gate dielectric layer;
patterning the first conductive layer and the gate dielectric layer to form an opening, wherein the opening exposes a predetermined surface of the substrate;
performing a first ion implantation process to form a doped region in the substrate under the exposed surface;
forming a second conductive layer over the substrate to fill the opening;
patterning the second conductive layer and the first conductive layer to form a gate of the reset transistor and a third conductive layer, wherein the third conductive layer has a first end extending over the isolation structure and covering a peripheral portion of the isolation structure, and wherein the third conductive layer has a second end extending to the active region of the substrate to be as a gate of a source follower transistor;
performing a thermal process to repair defects which occur on the sidewalls of the gate of the reset transistor and the third conductive layer, and drive the dopant of the doped region downward and then transversely diffuse them;
performing a second ion implantation process to form a lightly doped region in the substrate outside sidewalls of the gate;
forming a spacer respectively on the sidewalls of the gate of the reset transistor and the third conductive layer;
performing a third ion implantation process to form a heavily doped region in the substrate where a drain region is later formed; and
performing a thermal process to turn the lightly doped region and the doped region into a source region of the reset transistor, wherein the source region extends to the second well with second conductivity , and the heavily doped region and the lightly doped region form a drain region of the reset transistor.

[c9]

10.The process for producing the CMOS image sensor device of claim 9,

wherein a material of the gate dielectric layer is silicon oxide.

[c10] 11. The process for producing the CMOS image sensor device of claim 9, wherein the substrate is a P type silicon substrate.

[c11] 12.The process for producing the CMOS image sensor device of claim 9, wherein the first well with first conductivity is a P type well.

[c12] 13.The process for producing the CMOS image sensor device of claim 9, wherein the second well with second conductivity is a deep N type well.

[c13] 14.The process for producing the CMOS image sensor device of claim 9, wherein a material of the second conductive layer is a polycide.

[c14] 15.The process for producing the CMOS image sensor device of claim 9, further comprising a cleaning step to remove a native oxide and pollutants on the surface of the substrate, before forming a second conductive layer.

[c15] 16. The process for producing the CMOS image sensor device of claim 15, wherein a diluted hydrogen fluoride solution is used as a cleaning liquid in the cleaning step.